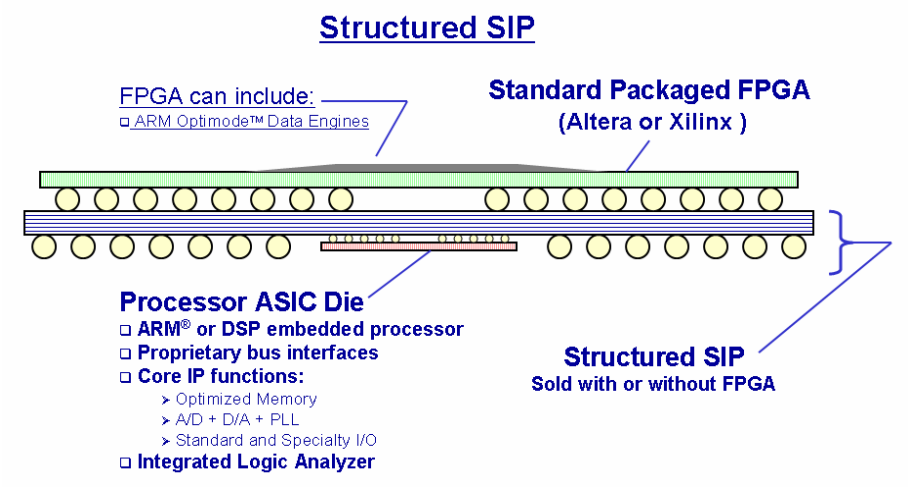
Faster Development for ARM and DSP Processor-Based ASICs
— Enabled by Structured SIP Technology —

Introduction

The following describes a new business opportunity for ARM partners - including ASIC suppliers, EDA companies and ASIC emulation and hardware development tool companies. This opportunity is based on a technology license for U.S. Patent No 7,062,744 that issued on June 13, 2006. The patent is entitled "Emulation solution for Programmable Instruction DSP", but was issued with claims broad enough to cover a Structured SIP/Emulator containing any ARM or DSP embedded processor.

A Structured SIP performs the function of the final embedded processor-based ASIC with the identical footprint. It consists of a custom substrate and a Processor ASIC which contains many commonly utilized functions. It also has provision to mount a standard *packaged* FPGA on top. It is an emulator you can ship.



ASIC Truths

There is a hole in the ASIC market, if you want to incorporate an ARM embedded processors:

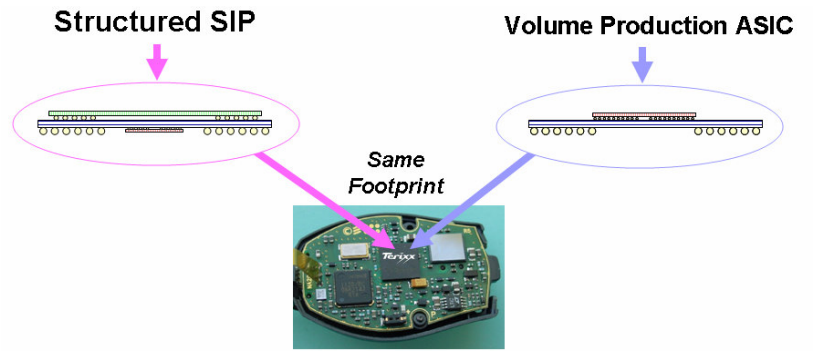
- Virtually all ASIC designs are initially prototyped with FPGAs.
- ARM supplies the majority (75%) of embedded processors in conventional ASICs.
- If you want to buy a current technology FPGA that includes an embedded, full-speed (hard) ARM processor (or a high performance, popular DSP) -- you can't !!!
- If you use Xilinx FPGAs, you may be tempted to use the on-board Power PC for ASIC prototypes and volume production.
- If you use Altera FPGAs, you are motivated to use their NIOS processor and HardCopy Structured ASICs, where there are essentially no license fees for volume production.
- Mask costs for Standard Cell SoCs continue to escalate, making Structured ASIC technology attractive and Platform ASICs (Structured SoCs) more viable.
- Product life cycles have shortened and time-to-market is more critical than ever.
- ASIC users must consider any product that shortens time-to-market and reduces development risk.

Benefits to Licensee

With ARM-based Structured SIPs available…

- …more ASIC customers start integration/debug sooner, find problems earlier, spin ASICs less, make their market window, and reach high volume production sooner.
- …more ASIC customers have prototypes in the final form factor sooner, start field trials sooner, find last minute problems sooner, spin ASICs less, make their market window, and reach their high volume potential.
- …ASIC users that prototype with Altera will have a higher performance alternative to NIOS in the ARM portfolio, and are less likely to take the all-Altera HardCopy path for volume production.
- …ASIC users that prototype with Xilinx will have an alternative to the Power PC, and a choice of ASIC foundry for volume production.
- The Processor ASIC netlist offers an additional IP licensing opportunity. It contains a number of IP blocks including memory, analog, and I/O functions in addition to an ARM core.
- Structured ASIC suppliers will be encouraged to offer Platform ASICs (Structured SoCs) based on ARM processors.

Structured SIP



Structured SIP products integrate full-speed (hard) ARM processors and memory with the latest FPGAs and Structured ASICs:

- Structured SIP devices with FPGAs...

  ...run at full processor speed
  ...fit the same form factor and footprint as the final ASIC
  ...can be shipped for early product field trials
  ...can be shipped in low volume production

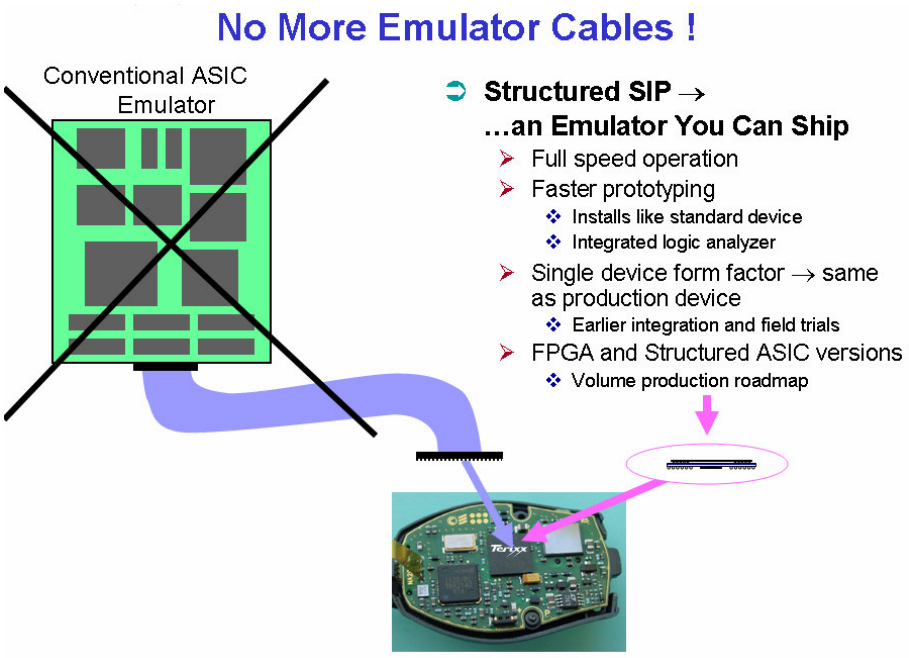
- Structured SIP devices with Structured ASICs...

  ...fit the same footprint as Structured SIPs w/FPGAs
  ...fit the same footprint as the final high-volume ASIC
  ...can be shipped in medium volume production

- Structured SIP devices provide the best path from FPGA to Platform ASICs (Processor + Structured ASIC)
- The fixed function portion (Processor ASIC) of the Structured SIP can be licensed for Platform ASICs and high-volume Standard Cell ASICs

No More Emulator Cables

Imagine putting hundreds of prototype systems into the hands of beta test customers months earlier than ever before. Then imagine finding a fatal problem during this early beta test that otherwise would have caused an ASIC spin and delayed production significantly. With conventional emulation prototypes, this scenario isn't possible!



Most ASIC users build emulation prototypes with FPGAs, and most of these prototypes are clumsy board based systems that take time and money to build. Sometimes, customers spend as much time debugging these systems as they do debugging their product. Also, most FPGA-based prototypes cannot be incorporated into the final form factor of the customer's product, which delays much of the testing that comes from field trials. Structured SIP devices fit the same footprint as the final production ASIC, and can be used in the final form factor of the ASIC developer's product.

Technology and Products

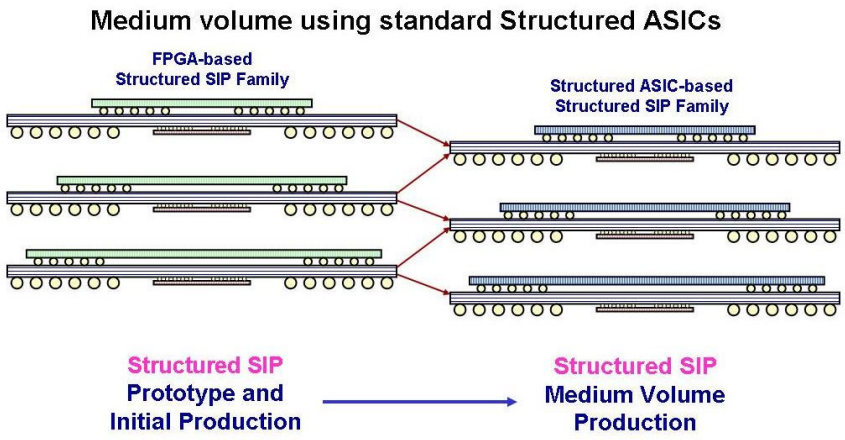
Structured SIP

A Structured SIP is a "System-In-Package" where two semiconductor devices are mounted to the same substrate. Together, they act like a single device and perform the function that the final ASIC device will perform. The Structured SIP is more than an emulator -- it has the same footprint that the final ASIC will have, enabling early integration and field trials, and even early production to test the target market.

Besides mating with popular packaged FPGAs, a Structured SIP can also mate with popular Structured ASICs (many Structured ASICs are designed to replace FPGAs already).

While Structured SIPs with FPGAs are only suitable for limited volume production, the use of Structured ASICs enables production to be ramped to a moderate volume level.

For high volumes, this methodology enables easy migration to either Platform ASICs or conventional Standard Cell-based ASICs. In either case, the netlist for the Processor ASIC is available for license.

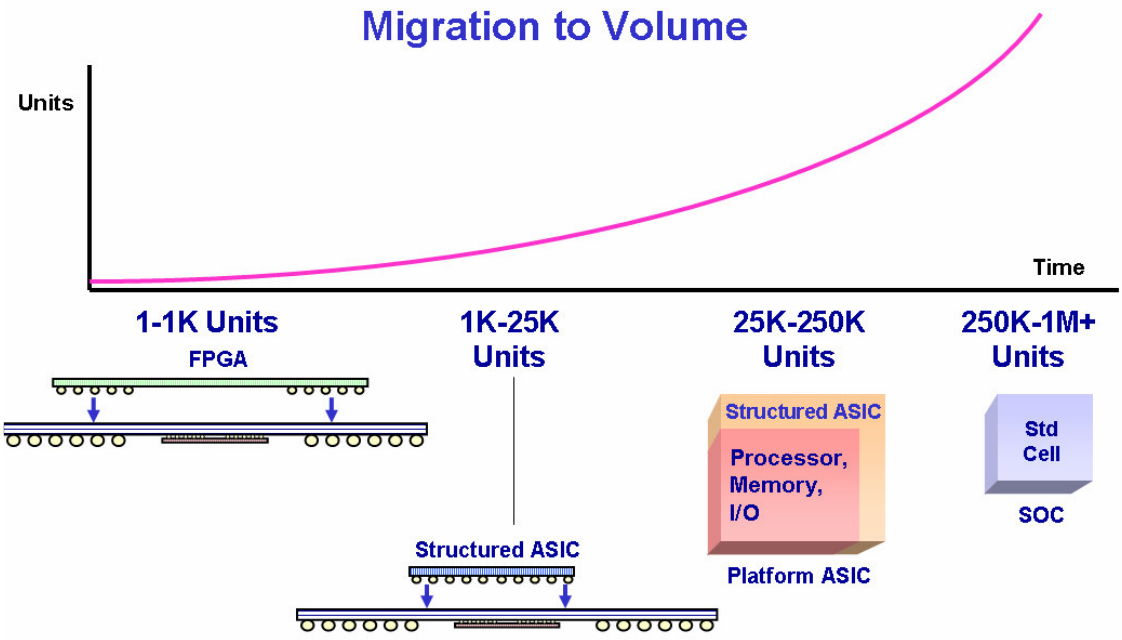


Platform ASICs

A "Platform ASIC" includes processor, memory, I/O, analog functions, and uncommitted logic constructed on the same die where the device can be customized with only a few custom masks. The uncommitted logic fabric is constructed with a "Structured ASIC" type of architecture, enabling much faster development, and a lower prototype cost due to significantly lowered mask costs.

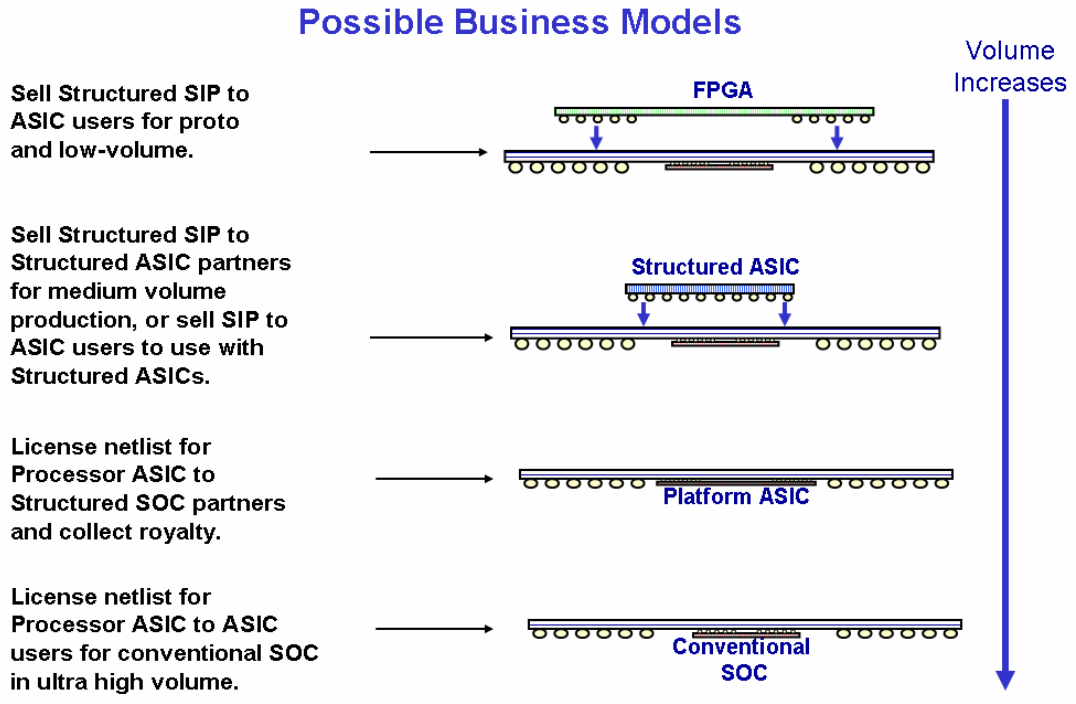
Conventional SoC

The Structured SIP methodology is a great insurance policy for conventional SoC development where finding problems earlier has the greatest return. Many problems are not found until full-speed hardware is available, and with Structured SIPs, this will happen many months sooner.



Business Models

A number of business models are possible, from selling the Structured SIP substrates to Licensing the netlist for the Processor ASIC. One or more of the models outlined below may be utilized by the licensee:



Summary

The availability of the Structured SIP solution provides a new revenue opportunity for ASIC suppliers, Development system and EDA software suppliers, or IP core suppliers. Designs that don't go to production or achieve disappointing volume levels due to late market entry will deliver greater volumes and total revenue or royalties. Designs that would have gone to ASIC vendors that don't support ARM will now go to ARM instead. Customers will save time and money due to fewer ASIC spins. Overall, Structured SIP is a win-win proposition for all involved.

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