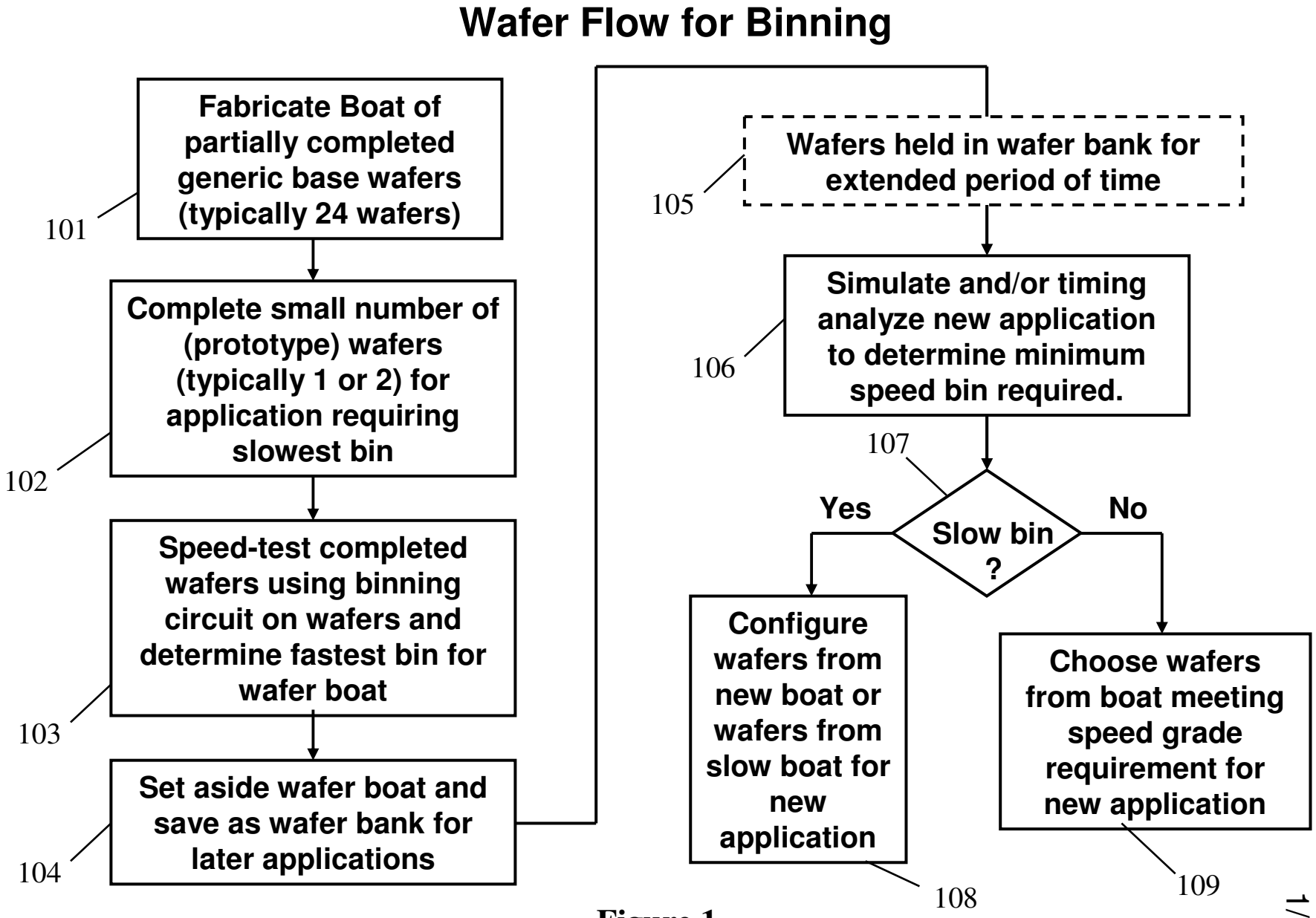

Figure 1

"Binning for Semi-Custom ASICs"
Robert Osann, Jr., 408-313-1990, Bob@Osann.com

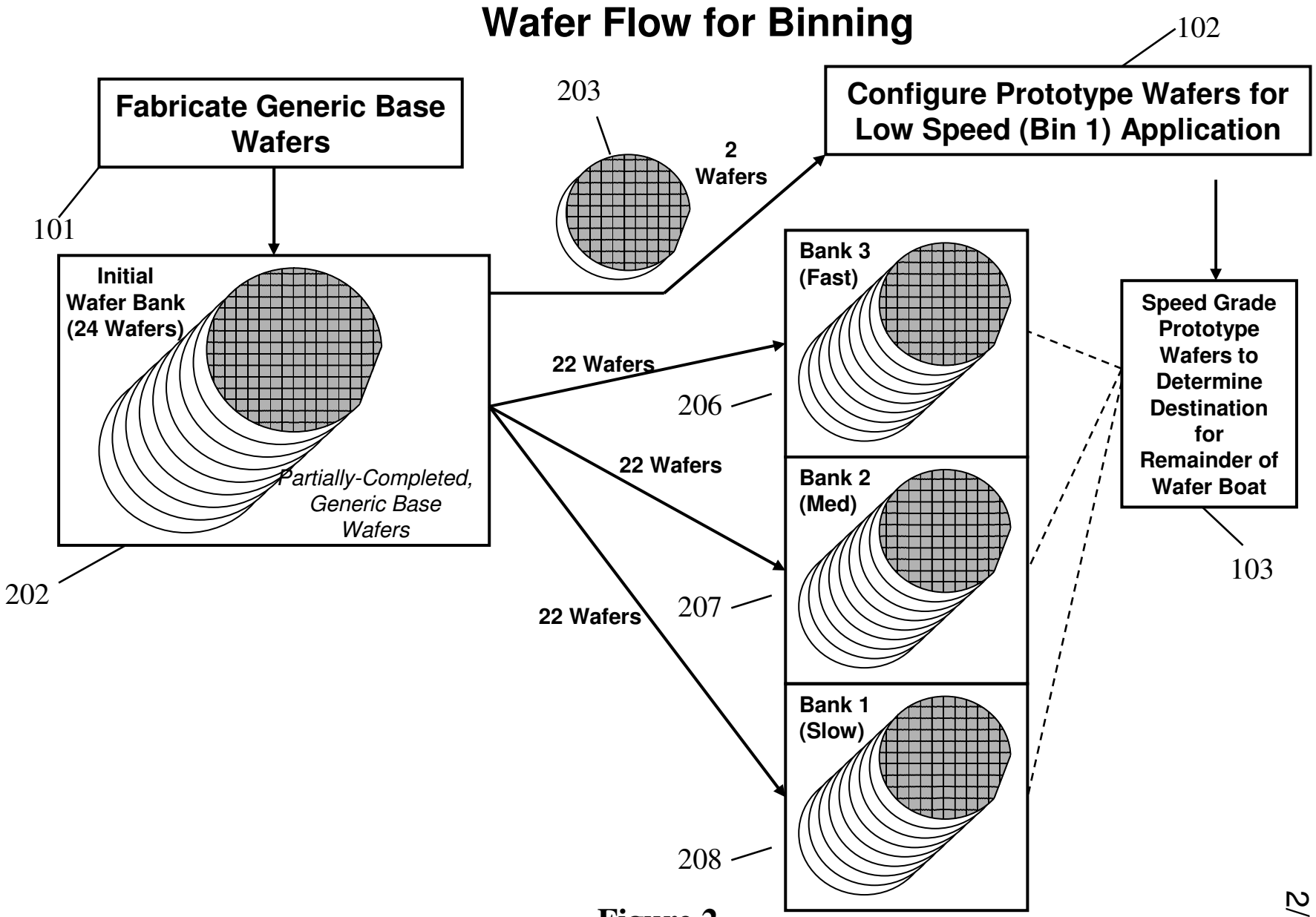
Wafer Flow for Binning
Fabricate Generic Base Wafers
101
Initial Wafer Bank (24 Wafers)
Partially-Completed, Generic Base Wafers
202
203
2 Wafers
Configure Prototype Wafers for Low Speed (Bin 1) Application
102
22 Wafers
22 Wafers
22 Wafers
206
207
208
Bank 3 (Fast)
Bank 2 (Med)
Bank 1 (Slow)
Speed Grade Prototype Wafers to Determine Destination for Remainder of Wafer Boat
103

Figure 2

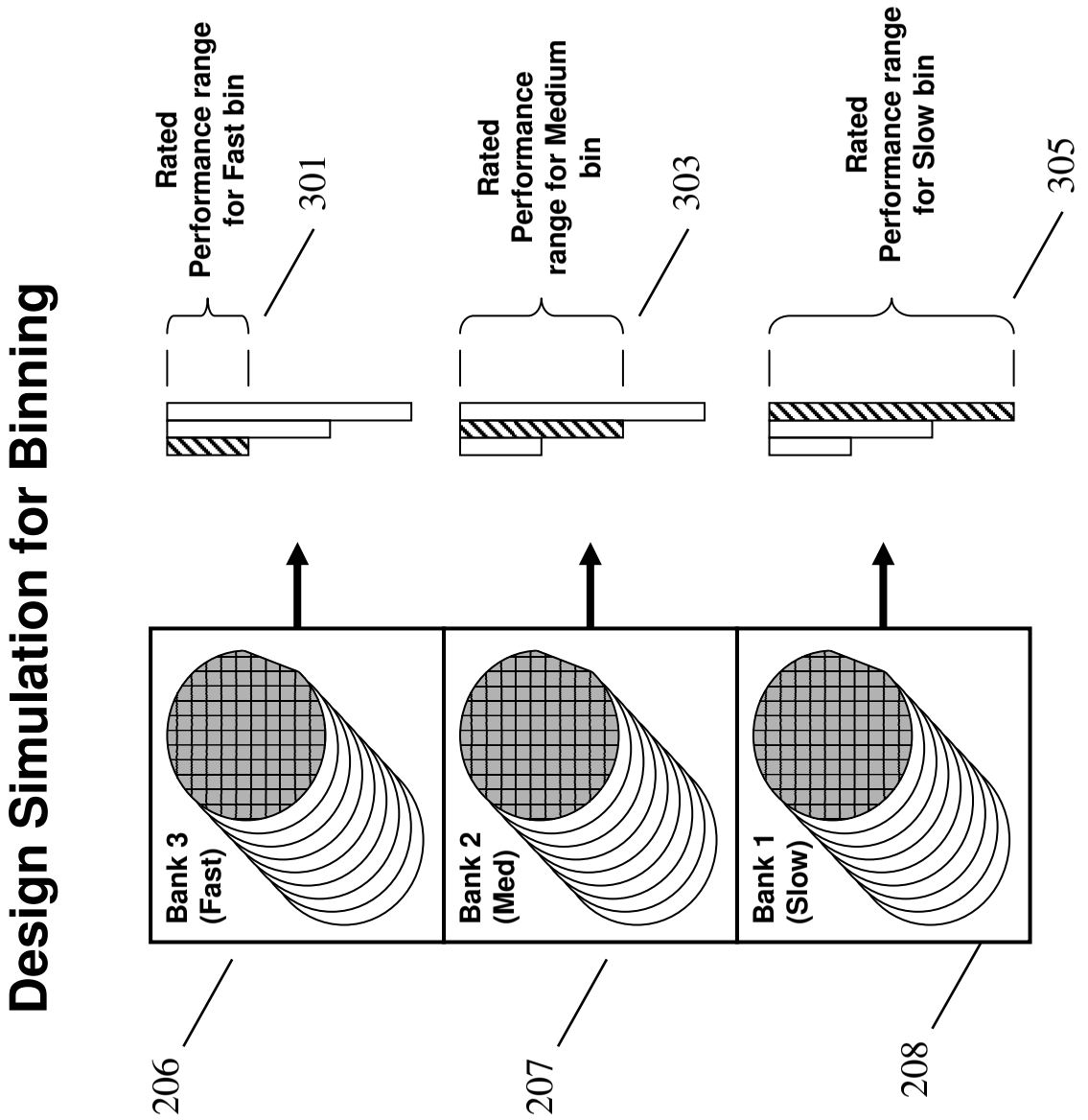
Design Simulation for Binning
Rated Performance range for Fast bin
301
Rated Performance range for Medium bin
303
Rated Performance range for Slow bin
305
Bank 3 (Fast)
Bank 2 (Med)
Bank 1 (Slow)
206
207
208

Figure 3

Performance Guardbands

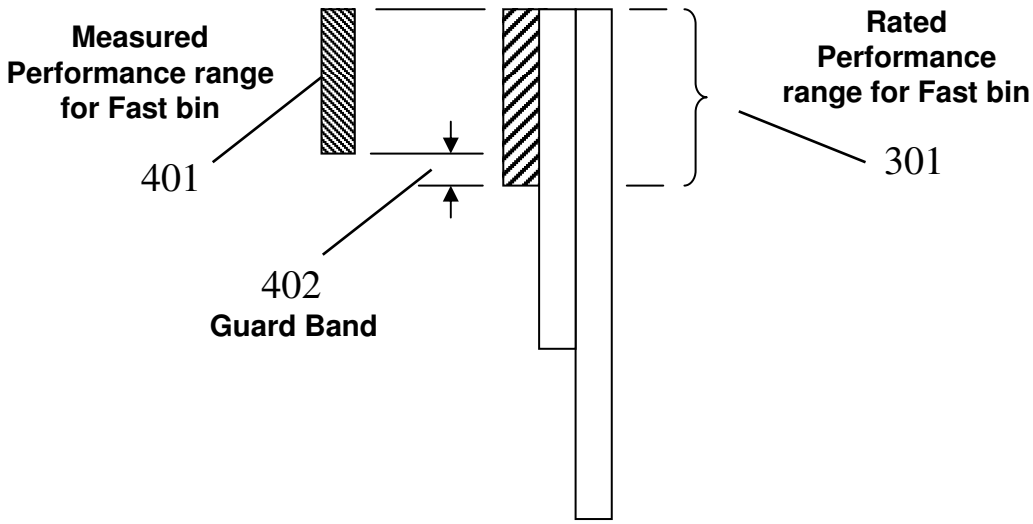

Figure 4