Silaero

Binning Structured ASICs

The first practical ASIC binning solution!

Introduction

Speed-grading (binning for speed) has been offered on standard components for decades. Even FPGAs which are field-customizable are offered at different performance levels, often providing up to a 35% increase in speed and selling at up to a 100% premium. Speed grading however has never been offered for mask-programmed ASICs. With Structured ASICs (module-based ASICs configured with a small number of custom masks) becoming more popular every day due to high mask costs, an opportunity now exists to offer speed grading for ASICs for the first time.

The solution described here is compatible with the operation of contemporary foundries and will enable ASIC vendors to offer performance increases on the order of 15% to 30% beyond what is available today on any process. Wafers can be binned for power consumption in a similar way using the method described. This exclusive process is described in US patent application number 10/704,850 filed on November 10, 2003.

History and Fab Issues

After creating the Structured ASIC at Lightspeed Semiconductor, the inventor of the ASIC binning methodology described herein was often frustrated by the fact that conventional ASIC devices were never offered with speed grading. In the late 90s, he filed a number of applications while at Lightspeed covering binning methodologies for structured ASICs which have since become the following US Patents:

6,133,582 Methods and apparatuses for binning partially completed integrated circuits based upon test results
6,399,400 Methods and apparatuses for binning partially completed integrated circuits based upon test results

Here, devices were fabricated up to a level where some but not all metal layers had been applied, however enough metal layers were constructed to connect transistors in order to form a functional binning circuit. The metal layers required to customize the device for a particular end-user application were yet to be applied.

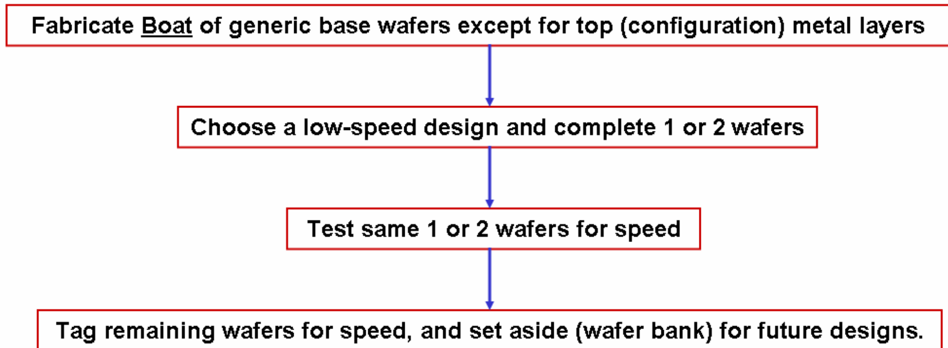
There was only one problem with these methods however. This was the requirement for partially completed wafers to leave the Fab area in order to be tested on the test floor, after which they would eventually have to be re-inserted into the Fab for the final metal layer processing steps to customize wafers for end-users. The operational procedures in contemporary Fabs unfortunately will not allow this to happen since once a wafer leaves the Fab, it may not enter the Fab again.

An "Outside the Fab" solution for ASIC binning

Wafers are typically processed in groups called "boats" which often contain 24 wafers. Wafers in the same boat tend to consistently exhibit similar levels of performance. Historically, a boat of wafers underwent most fabrication steps simultaneously in a "batch" mode. Although today some of these steps are now performed on wafers individually, even this individual processing is performed in the same timeframe on all wafers in a boat. The result is that wafers in a boat continue to exhibit similar performance. The method described

in US Patent App No 10/704,850 uses this phenomenon to assign performance characteristics - by inference - to partially configured wafers that have not yet been committed to any particular customer design. The method can also be used for binning other characteristics such as power consumption or leakage, and can be applied to other semi-custom devices such as conventional mask-programmed gate arrays (transistor arrays) in addition to Structured ASICs.

As described in the patent application, a boat of semi-custom ASIC wafers is fabricated to a partially-completed level where they are typically held in a "wafer-bank" while awaiting assignment to specific customer designs and applications. Wafers from a wafer bank may be split among many customer applications or all used for a particular customer. It depends on how many wafers are required to satisfy the needs of each customer.

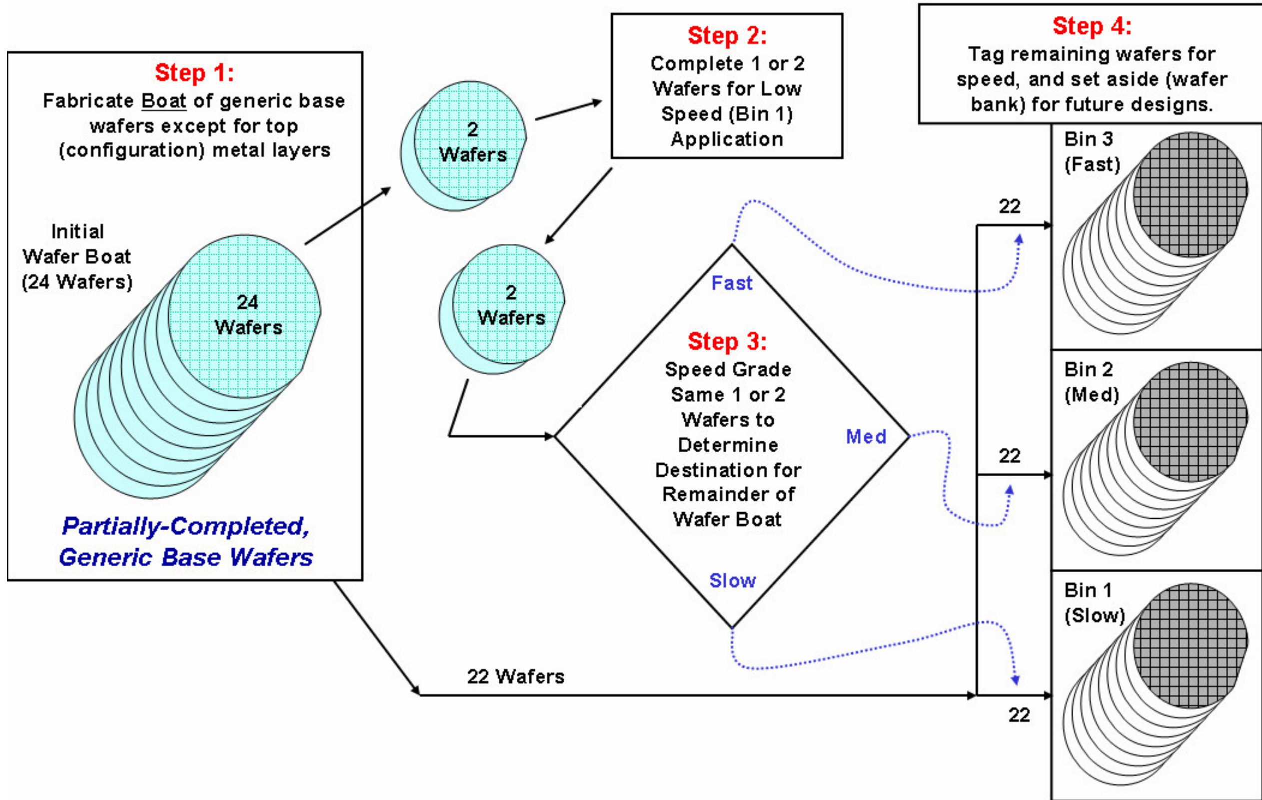


The key to this invention was to find a way to characterize the boat of wafers - prior to final customization - without taking them out of the Fab, and preferably without sacrificing any wafers in the process. This is accomplished by completing one or two wafers for use as prototypes for a specific customer design. As shown in this simplified diagram, a customer design is chosen which requires only the slow speed bin in order to operate successfully. This means that any speed, slow or fast, will support this first customer design successfully. So, when this first wafer or wafers are completed, they are tested for speed in order to determine how fast they really are even if the speed is in excess of the minimum requirement for the design. Based on this result, a speed grade is assigned to the remaining wafers in the boat - effectively by inference - and they are held in a wafer bank until customer designs requiring this particular bin or speed grade come along.

A diagram showing the wafer flow for this binning methodology is shown below, where the total number of wafers in a boat is shown, for example, as 24. Here, 2 wafers are taken to implement the initial customer design for a low-speed application, and the remaining 22 wafers are kept and effectively binned by inference based on the results of speed testing the initial 2 wafers. The remaining 22 wafers are shown in this diagram being assigned to one of three possible speed grades - slow, medium, or fast. Since the inferred speed grades may not provide the accuracy normally associated with speed testing of individual completed devices, a semiconductor process technology which would normally produce three or four speed grades may in fact only produce two or three speed grades when the methodology according to this invention is utilized. Even so, offering customers the option of increasing performance by 15-25% as opposed to a normal 30-35% is still of significant value since most ASIC designs seem to be marginal on their ability to meet customer performance requirements.

As mentioned earlier and other parameters may be binned besides speed. In particular, power consumption and leakage have become important parameters in recent years,

especially in the consumer space where battery power is more prevalent. Current leakage and power consumption can be binned according to the same methodology when semi-custom ASICs are the chosen implementation technology.



Summary

A binning solution has never been offered for mask-programmed ASIC devices. Using the fab-compatible methodology described here, such a solution can be offered - and for the first time!