Silaero

HYBRID-FPGA

APPLICATION-SPECIFIC EMBEDDED FPGA IN CONFIGURABLE DSP (rDSP™) APPLICATIONS

INTRODUCTION

DSPs are everywhere - they connect electronics to the real world. Conventional, high performance DSP devices sometimes fall short of required performance levels or require additional circuitry to interface with the system environment. In these cases, FPGAs or ASICs are often used with DSPs to accelerate specific algorithms and/or provide the required I/O interface capability.

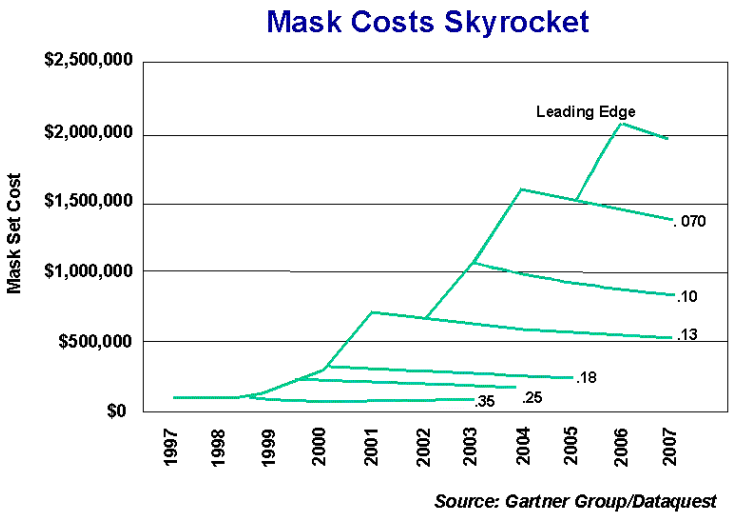
FPGA suppliers have embedded RISC processors hoping to address DSP as a primary market. This "Programmable SOC" strategy is falling short for DSP – it does not resonate with the DSP designer who is typically a software engineer with a degree in math. They want a true DSP. Also, FPGA technology is power consumptive and too expensive for volume applications.

Target Applications:

- **Algorithm Intensive**
- **TTM Sensitive**
- **Cost Sensitive**
- **Power Sensitive**

ASIC technology is used in dedicated DSPs like DVD, DSL, and MP3 – all high volume and time-to-market sensitive applications. At .13µ and beyond, development time is long and unpredictable, and mask costs are ~$1M. Conventional DSPs, could address more of these applications with the addition of selective algorithm acceleration and configurable I/O interfaces. A configurable platform is needed that offers more performance and I/O adaptability, while still providing low cost for high volume production. Hybrid-FPGA technology from Silaero will provide that solution.

Silaero has described and patented a breakthrough, configurable DSP platform for high volume applications that will enable DSPs to run faster and interface easily into OEM customer designs. Combined with a proven, high performance, multi-datapath DSP core, our unique "Hybrid-FPGA" technology will provide acceleration logic and I/O interfaces that can be altered by reprogramming devices in the field and from moment to moment. At the same time, these devices we call rDSP™ devices permit DSP programmers to program in the comfortable “C” code environment they are accustomed to.

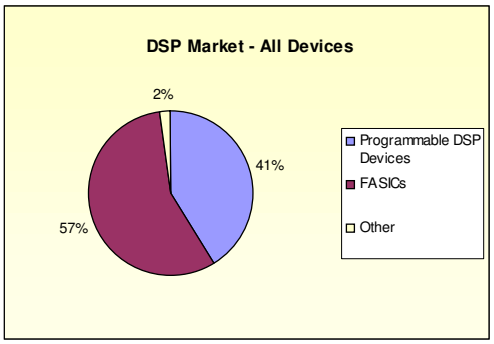


Source: Gartner Group/Dataquest

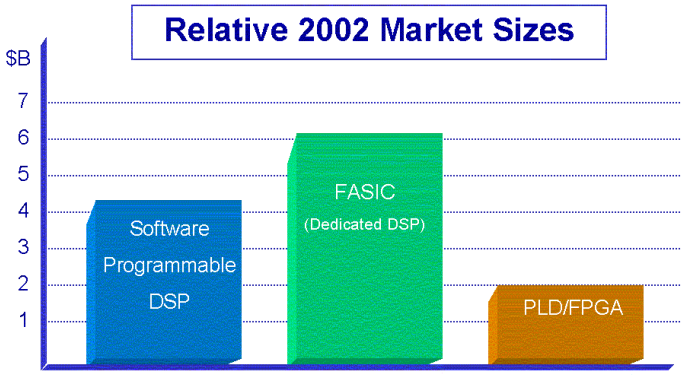
The rDSP™ approach provides the optimum DSP solution for "algorithm intensive" and time-to-market sensitive designs that demand high performance, flexibility, low power, and low device cost in high volume production. Initial applications will include those where video processing algorithms must be fine-tuned. rDSP™ devices will also find homes in applications for software defined radio and direct conversion receivers, to name only a few.

MARKET OPPORTUNITY

The opportunity is large for a company that can offer the highest performance, greatest flexibility, and lowest power and cost in a standard DSP device. The software programmable DSP device market has continued to grow at a reasonable rate.



An even larger market is represented by "dedicated" DSP devices called FASICs (Function and Algorithm Specific ICs) by Forward Concepts. This segment represents 57% of the total market for DSP devices of all types. rDSP™ devices will address opportunities in the FASIC segment when standards change or new application segments arise. Given the escalation in development cost and time starting at 0.13u and beyond, customers will increasingly adopt standard platforms that offer performance and flexibility benefits while avoiding the costs and delays associated with conventional SOC ASIC design. Combined, the traditional software programmable DSP market and dedicated DSP (FASIC) market dwarfed the PLD/FPGA market in 2002 and will continue to do so.



DSP APPLICATION PROFILE

Most software-programmable DSP applications have one characteristic that sets them apart form all other processor types - DSPs tend to spend most of their time executing a small number of instructions in a very tight loop. Often, this algorithm-intensive phenomena finds less than 10% of the code accounting for more than 90% of the execution time.

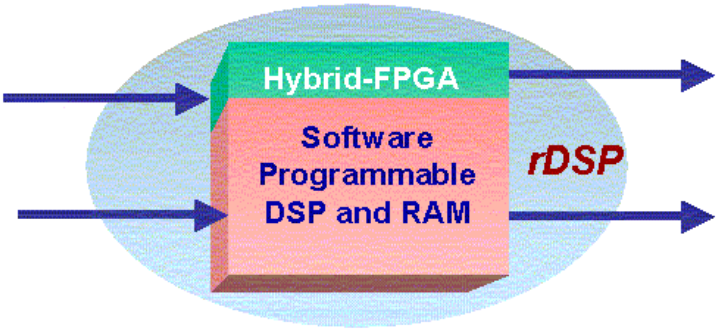
Engineers who design with DSPs are typically not hardware savvy. Mostly, they are software engineers with advanced degrees in math. Their expertise is in algorithms, and they prefer to design at an elevated level of abstraction - either in the "C" language or specifying algorithmic flow diagrams with tools like MATLAB. The are accustomed to programming conventional DSP Processors and that's what they want. Anything additional must be as non-intrusive as possible. Powerful, multi-datapath DSPs can perform as many as 8 multiplications at once, but they struggle when faced with complex bit-manipulation algorithms such as Viterbi decoders, Huffman encoding, and motion detection. In fact, TI has a standard DSP with a dedicated Viterbi decoder built-in to

address some of these issues. For these reasons, configurable hardware for selective acceleration will be especially valuable.

Flexibility is generally valuable in most DSP applications – not only in accelerating algorithms, but also in adapting to the myriad of I/O requirements placed on DSPs. A wide variety of serial and parallel I/O structures are encountered – some standard (like PCI) and many non-standard. Some are new and evolving, like serial video I/O. A strategy to deal with these requirements will extend the market reach of a configurable DSP platform well beyond what standard DSPs do today.

High volume dedicated DSPs (FASICs) using conventional ASIC technology have no flexibility once devices are delivered. FPGA technology could be added on-chip for flexibility, but at 4,000 gates/mm^2 on a 0.13u process, 50k to 100k gates of logic will destroy the cost effectiveness of the solution. Hybrid-FPGA technology will provide at least 5x the density of conventional FPGA and make configurability viable for high volume DSP applications.

A BETTER DSP SOLUTION - rDSP

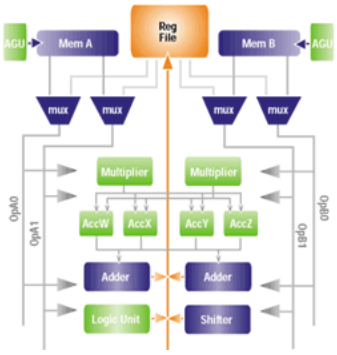


Reprogrammable DSPs

Hybrid-FPGA technology will add cost effective, high performance, and low power configurability to a conventional, high performance DSP architecture. These new devices overcome the shortfalls of existing DSP solutions – offering a practical degree of field-reprogrammability along with the ability to have complete configurability with only a few custom masks when required.

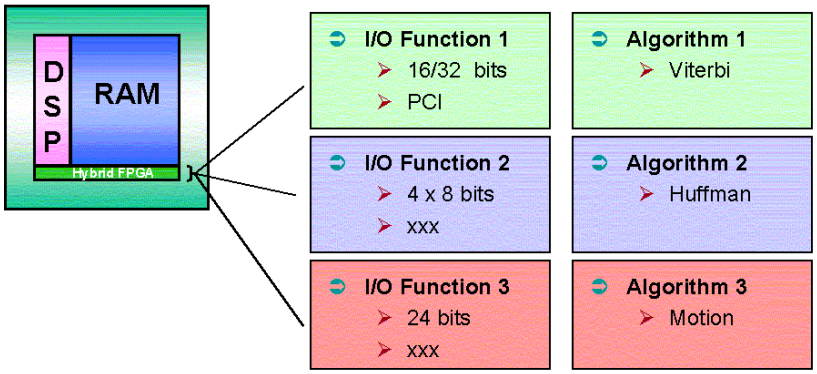
Proven DSP Core - Established Software Base

A complete solution will be based on a proven, high performance DSP processor core containing multiple arithmetic datapaths and having intrinsic performance equal to or better than today's standard DSP processor offerings. Suitable candidates include the next generation of Super-Scalar DSP architectures.



Multiple Personalities for I/O Functions and Selective Acceleration

Different DSP applications benefit from accelerating specific algorithms. Hybrid-FPGA technology will provide a group of selective acceleration personalities that can be chosen and also modified by reprogramming the device. Also designed for fast reconfiguration, personalities will occasionally be reprogrammed



"on-the-fly – further increasing the silicon efficiency of the solution.

Likewise, a family of I/O functionalities is provided where specific functions can be chosen and then modified through reprogramming the device.

Hybrid FPGA technology offers between 5x and 10X (tunable per application) the silicon density of conventional FPGA logic fabric on the same process technology. Thus, on a 0.09 micron process, three square millimeters of Hybrid-FPGA will provide at least 100,000 usable "ASIC" gates of logic.

One Device can Serve Many Applications
The chosen size for the Hybrid-FPGA area will cover the degree of flexibility and variation required for the initial target market segment. Applications that can be served by a single device, but require configurations beyond what reprogramming the Hybrid FPGA can accomplish, will be met with 4 or fewer metal layers of customization - avoiding the cost and unpredictably long development time of conventional SOC-based FASIC devices.

Higher Performance Customized Devices
Standard DSP processors from major suppliers are speed-graded to enable some devices to be sold at even higher performance levels (and margins). In the semiconductor industry, devices that utilize mask customization are never speed-graded. Silaero has created a proprietary methodology (patent pending) for binning Structured ASICs that enables not only reprogrammable devices to be speed-graded, but also devices that utilize limited mask customization (Structured ASIC technology), thereby extending their market reach. A Hybrid-FPGA structure using limited mask customization is supported by this patent application.

EXISTING DSP DEVICE SOLUTIONS
Software-programmable DSPs
These are conventional, software programmable processors with arithmetic function enhancements. The leading suppliers are TI and Analog Devices. The development environment is familiar to the DSP designer with code written mainly in “C”. Any modifications required for a design must be reprogrammed in software.

In the quest for higher performance, TI and other leading suppliers have added multiple arithmetic data path VLIW architectures, and even dedicated, application-specific functions. These "enhancements" are intended to increase performance for the 10% of the code that dominates execution time. For some algorithms, the ability to perform eight multiplications at once certainly increases performance. For other algorithms, conventional DSP architectures fall short.

Conventional DSPs usually have simple I/O interfaces. Often, however, the customer's application requires a more complex parallel or serial I/O functionality – sometimes matching an existing standard, sometimes not. The ability to meet a particular customer's interface requirement can make the difference between a high-volume design-in and not getting the business.

FASIC Devices - Dedicated DSPs

These are devices that are not programmable by the OEM – they are sold as fixed function, dedicated DSP devices. (Forward Concepts has coined the term "Function and Algorithm Specific ICs"). Example applications include DSL, DVD, MPEG, 802.11, and cable modems. Production volumes are typically very high and mostly focused on consumer applications. These are fast moving markets, and time-to-market is critical.

Often, these devices use a proprietary software-programmable DSP processor (with a fixed program) and an arithmetic ASIC fabric, all implemented on a Standard Cell SOC platform. While device costs in volume are extremely low, development time and cost are escalating rapidly. A platform solution providing fast time-to-market and low-cost high-volume production will penetrate many traditional FASIC applications.

Conventional DSPs + FPGA Devices

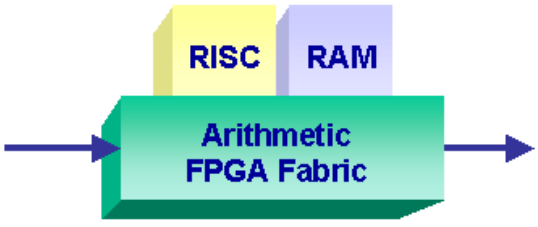
Sometimes, FPGAs are married discretely with DSPs to isolate compute intensive algorithms in the FPGA for hardware acceleration. This increases performance but has drawbacks regarding the development environment and device cost.

The large base of conventional DSP programmers prefer to design at a level of abstraction from the hardware. Introducing an FPGA device as part of the solution requires detailed hardware knowledge to partition the DSP functionality and integrate the FPGA and DSP together successfully. It is well known that this increases tool flow complexity, as well as the level of hardware knowledge and debugging skills required.

Increased cost occurs not only in team resources but in cost of goods as well. FPGAs are expensive! FPGAs by their nature are designed to suit a large application base - not being optimized for any particular application. FPGA vendors have tried to answer this endemic problem for DSP applications by sprinkling multipliers within some of their arrays. However, their base architectures were not designed with arithmetic functions in mind. Large amounts of general purpose, multi-port memory, as well as large multi-function I/O circuits, consume additional silicon area in FPGAs. In contrast, DSPs have specific memory and I/O requirements.

Embedded RISC in FPGA

In recent years, FPGAs have been enhanced in an effort to increase their effectiveness in DSP applications, initially by adding dedicated multipliers to the existing programmable logic fabric. Some FPGAs now contain RISC processors, not specifically for DSP, but for any application where a processor adds value. However, the RISC processor is subordinate to the FPGA. The devices are first and foremost, FPGAs.



Typical FPGA Use Paradigm

A different paradigm is required to effectively address the DSP device markets. To fit the

development environment desired by DSP designers, the configurable fabric must be subordinate to the software-programmable DSP. And, the processor must be a real DSP, not a RISC!

rDSP BENEFITS:

- Significant performance increase in selected applications
- Configurable I/O Interfaces
  - Adapt to specific customer application
- Familiar DSP processor paradigm
  - Standard "C" coding environment or MATLAB interface
- Proven DSP core with extensive software support
- Low-cost high volume production
  - Programmable fabric 5x FPGA density
- Similar power consumption to conventional DSP

rDSP Solution compared to the DSP solution landscape:

	Additional Performance over DSP	Early Hardware Verification	Familiar Develop-ment Paradigm	Configurable I/O Interfaces	Low cost in volume production	Low Development Cost
Conventional DSP	**no**	**yes**	**yes**	**no**	**yes**	**yes**
rDSP	**yes**	**yes**	**yes**	**yes**	**yes**	**yes**
Processor + FPGA	**yes**	**yes**	**no**	**yes**	**no**	**yes**
Conventional FASIC	**yes**	**no**	**no**	**no**	**yes**	**no**

INTELLECTUAL PROPERTY

As of November 2006, one patent on Hybrid-FPGA has been issued (7,093,225) covering the embodiment that utilizes Structured ASIC methods for the mask-configuration steps. A Divisional application (A/N 11/474,876 - not yet published) has also been filed to cover constructing a Hybrid-FPGA using full-custom or Standard Cell techniques. Our application for Binning Structured ASICs (A/N 10/704,850) is applicable to US Pat 7,093,225 but has not been published on the PTO site. Our method for emulating embedded processor applications is described in recently issued US Patent No 7,062,744 where a System in Package (SIP) structure is used with conventional FPGAs (or Structured ASICs) to emulate the volume production device and also be shipped in low to medium volume production.

SUMMARY

Hybrid FPGA technology provides the right combination of performance and flexibility for tackling ever-changing customer design requirements in embedded processor applications - especially DSP. Embedded FPGA has been attempted in ASICs and has always been abandoned due performance and die size - most of all die size - considerations.

The goal is to meet and exceed the customer's application performance metric, while providing the flexibility required in a diverse market that often requires algorithm tweaking and changing. Tightly coupled with a conventional DSP processor, our Hybrid-FPGA solution will better enable designers to differentiate and add value to their products, as well as meet evolving standards. In addition, the unique ability of the architecture to provide configurable I/O functions is both important to manage the sheer number of chip combinations and to enable selling into a diverse market space.